CLAIMS

WHAT IS CLAIMED:

1. A method, comprising:

receiving a command from a controller to access a memory;

receiving, from the controller, at least one of burst length information and latency information in association with the command to access the memory; and

providing data to or from the memory in response to the command based on at least one of the burst length information and the latency information.

2. The method of claim 1, wherein receiving a command comprises receiving at least one of a READ operation and WRITE operation to access the contents of the memory.

3. The method of claim 2, wherein receiving the latency information comprises receiving at least one of column address strobe latency information and write latency information.

4. The method of claim 1, wherein receiving at least one of the burst length information and the latency information in association with the command to access the memory comprises receiving at least one of the burst length information and the latency information substantially contemporaneously with the command to access the memory.

5. The method of claim 1, wherein receiving the burst length information comprises receiving a burst length information based on an amount of data to be retrieved from the memory.

6. The method of claim 4, wherein receiving the burst length information comprises receiving a burst length of a first preselected value in response to the controller receiving a request from a peripheral client and a burst length of a second preselected value in response to the controller receiving a request from a main client, wherein the first preselected value is less than the second preselected value.

7. The method of claim 1, wherein receiving at least one of the burst length information and latency information comprises receiving the information over a redundant address line to the memory.

8. The method of claim 7, wherein receiving the information over the redundant address line comprises receiving the information over a redundant row address line.

9. The method of claim 7, wherein receiving the information over the redundant address line comprises receiving the information over a redundant column address line.

10. An apparatus, comprising:

a controller adapted to:

provide a command to access a memory array;

provide at least one of burst length information and latency information in association with the command to access the memory array; and

receive data from the memory array in response to the command based on at least one of the burst length information and the latency information.

11. The apparatus of claim 10, wherein the controller is adapted to issue a READ operation access the contents of the memory.

12. The apparatus of claim 10, wherein the controller is adapted to provide at least one of the burst length information and the latency information substantially contemporaneously with the command to access the memory.

13. The apparatus of claim 10, wherein the controller is adapted to provide a burst length of a first preselected value in response to receiving a request from a peripheral client and a burst length of a second preselected value in response to receiving a request from a main client, wherein the first preselected value is less than the second preselected value.

14. The apparatus of claim 10, wherein the controller is adapted to provide at least one of the burst length information and latency information over a redundant address line to the memory.

15. The apparatus of claim 14, wherein the controller is adapted to provide at least one of the burst length information and latency information over at least one of a redundant column address line and a redundant row address line.

16. The apparatus of claim 10, wherein the controller is adapted to issue a WRITE command and adapted to provide write latency information substantially contemporaneously with the WRITE command.

17. A system, comprising:

a memory array, and

a controller communicatively coupled to the memory array, the controller adapted to:

provide a command to access the memory array; and

provide at least one of burst length information and latency information in association with the command to access the memory array; and

wherein the memory array is adapted to provide or receive data in response to the command based on at least one of the burst length information and the latency information.

18. The system of claim 17, wherein the controller is adapted to issue at least one of a READ operation and WRITE operation access the contents of the memory.

19. The system of claim 17, wherein the controller is adapted to provide at least one of the burst length information and the latency information substantially contemporaneously with the command to access the memory.

20. The system of claim 17, wherein the controller is adapted to provide a burst length of a first preselected value in response to receiving a request from a peripheral client and a burst length of a second preselected value in response to receiving a

request from a main client, wherein the first preselected value is less than the second preselected value.

21. The system of claim 17, wherein the controller is adapted to provide at least one of the burst length information and latency information over a redundant address line to the memory.

22. An apparatus, comprising:

means for providing a command from a controller to access a memory;

means for providing, from the controller, at least one of burst length information and latency information in association with the command to access the memory; and

means for providing data to or from the memory in response to the command based on at least one of the burst length information and the latency information.

23. An apparatus, comprising:

a memory adapted to:

receive a command from a memory controller to access contents of the memory;

receive, from the memory controller, at least one of burst length information and latency information in association with the command to access the contents; and

provide data from the memory in response to the command based on at least one of the burst length information and the latency information.

24. The apparatus of claim 23, wherein memory is adapted to receive at least one of the burst length information and the latency information substantially contemporaneously with the command to access the memory.

25. The apparatus of claim 23, wherein the memory is adapted to receive a burst length of a first preselected value in response to the controller receiving a request from a peripheral client and a burst length of a second preselected value in response to the controller receiving a request from a main client, wherein the first preselected value is less than the second preselected value.

26. The apparatus of claim 23, wherein the memory is adapted to receive at least one of the burst length information and latency information over a redundant address line.

27. The apparatus of claim 26, wherein the memory is adapted to receive at least one of the burst length information and latency information over at least one of a redundant column address line and a redundant row address line.

28. The apparatus of claim 23, wherein the memory is adapted to receive a WRITE command and adapted to receive write latency information substantially contemporaneously with the WRITE command.